**Akhila P** **Email:** akhila.btech18@gmail.com

 **Contact No**:+91- 9848984197.

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**CARRIER OBJECTIVE:**

Always seeking innovative and challenging career in the professionally managed and dynamic organization, which provides the best opportunities for the development and greater responsibilities to contribute towards organization.

**SUMMARY:**

* Keen in learning Web Technologies.
* Hands on Core java and OOPS concepts.
* Having good knowledge on Database like ORACLE, MY SQL.
* Interested to learn new technologies. Adapt easily to new environment.
* Hands on Manual Testing and Automation.

**EDUCATIONAL QUALFICATION:**

* **B. Tech\***(Electronics and Communication Engineering) with aggregate 70% in 2014-2018from S.K.D Engineering Gooty.
* **12th**with aggregate 80%from Narayana Junior Collage from Anantapur in 2014.
* **10th**with aggregate 8.8 GPA (Scale of 10.0) from C.K.K.Memory school in 2012.

**TECHNICAL SKILLS:**

**Languages :** C,JAVA

**Testing :** Manual Testing, Agile

**Database** : SQL,ORACLE

**Web Technologies :** HTML, CSS, JAVA SCRIPT

**ACADEMIC PROJECT:**

**Title:**

 **Design and Implementation of FPGA based 64-bit MAC Unit using VEDIC Multiplier and Reversible Logic Gates.**

**Description:**

Now a days in VLSI technology size, power, and speed are the main constraints to design any circuits. In normal multipliers delay will be more and the number of computations also will be more. Because of that speed of the circuits designed with the normal multipliers will be low and it will consume more power. This paper describes multiply and Accumulate Unit using Vedic Multiplier and DKG reversible logic gates. The Vedic multiplier is designed by using Urdhava Triyagbhayam sutra and the adder design is done by using reversible logic to perform high speed operations. Reversible logic gates are also the essential constraint for the promising field of Quantum computing. The Urdhava Triyagbhayam multiplier is used for the multiplication function to reduce partial products in the multiplication process and to get high concert and less area. The reversible logic is used to get less power. The MAC is designed using Verilog code, simulation, synthesis is done in both RTL compiler using Xilinx and implemented on Spartan 3e FPGA Board.

**Project Keywords**

MAC, Reversible Gates, Vedic Multiplier

**STRENGTHS:**

* Good coding sills
* Determined to learn with practical approach
* Good communication skills
* Enthusiastic and can produce results under deadline constraints.

**ACHIVEMENTS:**

* Certified in Java and Testing.
* Taken part in workshops held in JNTU Anantapur.
* Elected as Leader of Class.

**PERSONAL DETAILS:**

 Father’s Name : P.Sudhakar Reddy

 Mother’s Name : P.Nageswaramma

 Date of Birth : 8th April 1997

 Marital Status : Single

 Languages known : Telugu, English, Hindi

 Current location : Bangalore

 Contact No : 984894197

 Permanent Address : Gooty, Anantapur, A.P-515401

**DECLARATION:**

 I hereby declare that all the above facts are true to best of my knowledge.

 (**P.Akhila Reddy**)